## CLAIMS

1. A method of storing failure addresses of a memory cell, said method comprising the steps of:

storing an address and corresponding fail count for a plurality of cells of said memory cell in a register until said register is full;

determining if a plurality of cells in an input register has a greater fail count than a fail count of a plurality of cells currently stored in said register; and

replacing said address and a corresponding fail count in said register with said address and corresponding fail count in said input register if the fail count of said plurality of cells in said input register is greater than said fail count of said plurality of cells currently stored in said register.

2. The method of claim 1 wherein said step of determining if a plurality of cells in an input register has a greater fail count than a fail count of a plurality of cells currently stored in said register comprises determining if a row in said input register has a greater fail count than a fail count of any row currently stored in said register.

3. The method of claim 2 wherein said step of replacing said address and a corresponding fail count in said register comprises replacing a currently stored row address and a corresponding fail count with a row address and corresponding fail count from said input register.

4. The method of claim 3 further comprising a step of replacing said rows stored in said register with redundant rows.

5. The method of claim 1 wherein said step of determining if a plurality of cells in an input register has a greater fail count than a failure count of a plurality of cells currently stored in said register comprises determining if a column in said input register has a greater fail count than a failure count of any column currently stored in said register.

6. The method of claim 1 wherein said step of replacing said address and a corresponding fail count in said register comprises replacing said currently stored column address and a corresponding fail count with a column address and corresponding fail count in said input register.

7. The method of claim 7 further comprising a step of replacing said columns stored in said register with redundant columns.

8. A method of storing failure addresses of a memory cell, said method comprising the steps of:

storing a plurality of addresses and corresponding fail counts for a plurality of rows in a register until said register is full;

loading a new row address and a corresponding fail count into an input register;

simultaneously comparing said corresponding fail count of said new row address to said plurality of fail counts stored in said register; and

replacing a row address and a corresponding fail count in said register if the corresponding fail count of said new address is greater than a fail count corresponding to said row address stored in said register.

9. The method of claim 8 further comprising a step of storing a plurality of addresses and corresponding fail counts for a plurality of columns in a register until said register is full.

10. The method of claim 9 further comprising a step of loading a new column address and a corresponding fail count into an input register.

11. The method of claim 10 further comprising a step of simultaneously comparing said corresponding fail count of said new column address to all stored fail counts.

12. The method of claim 11 further comprising a step of replacing a column address and a corresponding fail count in said register if the corresponding fail count of said new column address is greater than a fail count of a column address stored in said register.

13. The method of claim 12 further comprising steps of repeating said steps of replacing a row address and a corresponding fail count in said register if the corresponding fail count of said new row address is greater than a fail count of a row address stored in said register and replacing a column address and a corresponding fail count in said register if the corresponding fail count of said new column address is greater than a fail count of a column address stored in said register.

14. The method of claim 13 further comprising a step of replacing said column addresses stored in said register with redundant column addresses.

15. A method of storing failure addresses of a memory cell, said method comprising the steps of:

storing a plurality of row addresses and corresponding failure counts for rows in a register until said register is full;

loading a new row address and a corresponding fail count into an input register;

sequentially comparing said corresponding fail count of said new fail address to all stored fail counts in said register; and

replacing a row address and a corresponding failure count in said register if the corresponding fail count of said new row address is greater than a failure count of said row stored in said register.

16. The method of claim 15 further comprising a step of storing a plurality of addresses and corresponding fail counts for a plurality of columns in a register until said register is full.

17. The method of claim 16 further comprising a step of loading a new column address and a corresponding fail count into an input register.

18. The method of claim 17 further comprising a step of simultaneously comparing said corresponding fail count of said new column address to all stored fail counts.

19. The method of claim 18 further comprising a step of replacing a column address and a corresponding fail count in said register if the corresponding fail count

of said new column address is greater than a fail count of a column address stored in said register.

20. The method of claim 19 further comprising steps of repeating said steps of replacing a column address and a corresponding fail count in said register if the corresponding fail count of said new column address is greater than a fail count of a column address stored in said register and replacing a row and a corresponding fail count in said register if the corresponding fail count of said new column address is greater than a fail count of a column stored in said register.

21. The method of claim 20 further comprising a step of replacing said columns stored in said register with redundant columns.

22. A memory device having a register storing failure addresses, said memory device comprising:

an input register receiving an input fail address and an input fail count;

a register having a plurality of slots storing fail addresses and corresponding fail counts; and

a plurality of comparators, each said comparator being coupled to said input fail count and a fail count of one of said slots of said registers.

23. The memory device of claim 22 further comprising a clock signal.

24. The memory device of claim 23 further comprising a switch coupled to said clock signal, said switch providing said input fail address and said input fail count to a slot of said register.

25. The memory device of claim 24 wherein said switch closes on a falling edge of said clock signal.

26. The memory device of claim 22 further comprising a plurality of register switches, each register switch of said plurality of register switches being coupled to receive an output of a comparator of said plurality of comparators.

27. The memory device of claim 26 wherein each said register switch of said plurality of register switches being coupled to a slot of said plurality of slots of said register.

28. The memory device of claim 22 wherein said plurality of comparators are coupled said clock signal, each said comparator being enabled on a rising edge of said clock signal.

29. A memory device having a register storing failure addresses, said memory device comprising:

an input register receiving an input fail address and an input fail count;

a register having a plurality of slots storing fail addresses and corresponding fail counts;

a plurality of comparators, each comparator being coupled to an input fail count and a fail count of one of said slots of said register;

a switch coupled to a clock signal, said switch providing said input fail address and said input fail count to a slot of said register; and

a plurality of register switches, each register switch being coupled to receive an output of a comparator of said plurality of comparators.